

Mohamed Zahran

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- EDUCATION
- ◇ **University of Maryland**, College Park, MD.
Ph.D. in Electrical and Computer Eng., May 2003
Dissertation Title: “Hierarchical Multithreading Architecture”
Adviser: Prof. Manoj Franklin GPA = 3.9/4.0
 - ◇ **Cairo University**, Egypt.
M.Sc. in Computer Engineering, July 1999.
Thesis title: “A New Adaptive Genetic Algorithm”
 - ◇ **Cairo University**, Egypt.
B.Sc. in Computer Engineering, July 1997.
Graduation Project: “Computer Chess”
- RESEARCH INTERESTS
- ◇ **Memory hierarchy design for manycore processors**
 - ◇ **Brain-inspired microprocessor design**
 - ◇ **Hardware-software interaction**
 - ◇ **Hardware support for trusted platforms**
 - ◇ **Power-aware computing**
 - ◇ **High performance computing**
- WORK EXPERIENCE
- ◇ **New York University** (Aug 2010 - present)
Faculty with Computer Science Department, Courant Institute of Mathematical Sciences, NYU
 - ◇ **Consultancy Work** (2007-2010)
 - Polytechnic Institute of NYU:
 - Designing power-efficient supercomputer based on hybrid FPGA and general purpose processors using switched networks.
 - Architecture support for Trusted Platform Management for single core, multicore, and manycore processors.
 - Cairo Microsoft Innovation Center (CMIC):
Proposed and supervised research projects related to high-performance computing. The projects I have contributed to are related to parallelization and analysis of bioinformatics applications.
 - ◇ **City University of New York - City College** (Sep 04 - May 10)
Department of Electrical Engineering and the Computer Engineering program,
Assistant Professor (Sep 04 - Aug 09), then Adjunct Associate Professor (Sep 09 - May 10)
 - ◇ **The George Washington University** (Sep 03 - Jul 04)
Research Scientist with the Department of Electrical and Computer Engineering.
Duties included directing two groups of graduate students:
 - The first group did research on the specifications and performance of a parallel version of the C language, called unified parallel C (UPC).
 - The second group focused on reconfigurable architecture, and how to dynamically reconfigure a device to adapt to program(s) behavior.
 - ◇ **University of Maryland at College Park**

Mohamed Zahran

- Research Assistant (Aug 99 - Aug 03):
Department of Electrical and Computer Engineering
Research topic: The Microarchitecture of Speculative Multithreaded Processors.
- Teaching Assistant (Aug 99 - May 2001):
Department of Electrical and Computer Engineering
Assisted in teaching: Digital Logic Design, Computer Organization.
Duties: holding weekly recitation classes, office hours as well as grading homework assignments and exams.

◇ **Cairo University, Egypt** (Sep 97 - May 99)

Assistant Lecturer:

Teaching: C programming language, Digital Logic Design,
Computer Architecture, Software Engineering and Operating Systems.

◇ **American University in Cairo (AUC)** (Spring 98)

Lecturer:

Center of Adult and Continuing Education (CACE),
Duties: Teaching computer architecture and assembly language programming course.

◇ **IBM Egypt** (Summer 96)

Summer Intern:

Performance analysis and tuning of IBM RISC/6000.

◇ **AT&T Global Information System, Egypt**

Summer Intern:

- (Summer 95): UNIX operating system and Unix Shell programming workshops, Data communication and LAN and WAN concepts workshops.
- (Summer 94): Windows applications workshop, C programming language and Clipper application workshops.

HONORS AND AWARDS ◇ Best Poster Award in Trusted Infrastructure Workshop (TIW), June 2010.

- ◇ First place in ACM Student Research Competition with my Ph.D student Bushra Ahsan, held in the 18th International Conference on Parallel Architectures and Compilation Techniques (PACT) 2009.
- ◇ Elected Senior member of ACM.
- ◇ Elected Senior member of IEEE.
- ◇ Certificate of Recognition at City University of New York on the occasion of the “Salute to Scholars” event in Dec 2008 in honor of outstanding scholarly achievements.
- ◇ Top three nationwide (second place) in ACM Student Research Competition with my undergraduate student Jerry Backer, 2007.
- ◇ Awarded grant from IBM to attend 39th International Symposium on Microarchitecture (MICRO), 2006.
- ◇ Awarded grant from ACM SIGARCH for young faculties to attend International Conference on Microarchitecture, held in Oregon, December 2004.
- ◇ Best paper award in International Conference on Computer Design (ICCD), San Jose, CA, October, 2003.
- ◇ ACM/SIGARCH conference student grant award: ISCA/FCRC 2003

Mohamed Zahran

- ◇ Best Graduate student scientific talk in Electrical and Computer Engineering dept., University of Maryland, fall 2002.
- ◇ Honors with Distinction (First Place) in University of Maryland Graduate Research Interaction Day (GRID), 2002.
- ◇ Honors with Distinction at M.Sc (top 5), Cairo University, 1999.
- ◇ Honors with Distinction at B.Sc, Cairo University 1997.
- ◇ Scholarship during all undergraduate studies, Cairo University, Egypt (fall 92 - summer 97), given only to B+ and higher GPA.

PUBLICATIONS **Refereed Papers:**

1. Arun K. Kanuparthi, **Mohamed Zahran**, and Ramesh Karri, *Architecture Support for Dynamic Integrity Checking*, IEEE Transactions on Information Forensics and Security (to appear).
2. Corey Malone, **Mohamed Zahran**, and Ramesh Karri, *Are Hardware Performance Counters a Cost Effective Way for Integrity Checking of Programs?*, The Sixth ACM Workshop on Scalable Trusted Computing, October 2011.
3. Artem Durytskyy, **Mohamed Zahran**, and Ramesh Karri, *Improving Robustness of GPUs by Making Use of Faulty Parts*, Proc. International Conference on Computer Design (ICCD11), October 2011.
4. Mohamed Salah Souahi, Smail Niar, **Mohamed Zahran**, Mohamed Benmohamed, *Towards Dynamic Cache Block Placement for Multi-processor NUCA*, IEEE International Conference on Microelectronics, December 2011.
5. Arun K. Kanuparthi, **Mohamed Zahran**, and Ramesh Karri, *Feasibility Study of Dynamic Trusted Platform Module*, Proc. International Conference on Computer Design (ICCD10), October 2010.
6. Ahmed Youssef, **Mohamed Zahran**, Mohab Anis, and Mohamed Elmasry, *On the Power Management of Simultaneous Multithreading Processors*, IEEE Transactions on VLSI Systems, pp. 1243-1248, Vol. 18, August 2010.
7. **Mohamed Zahran** and Sally A. McKee, *Global Management of Cache Hierarchies*, The ACM International Conference on Computing Frontiers (CF'10), Italy, May 2010.
8. Yufu Zhang, Ankur Srivastava, and **Mohamed Zahran**, *On-Chip Sensor Driven Efficient Thermal Profile Estimation Algorithms*, ACM Transactions on Design Automation of Electronic Systems, Volume 15 , Issue 3, May 2010.
9. Najla Alfaraj, H. Jonathan Chao, and **Mohamed Zahran**, *NBC: Network-based Cache Coherence Protocol for Multistage NoCs*, in The International SoC Design Conference (ISOC), 2009.
10. Kim Hazelwood and **Mohamed Zahran**, *Challenges and Opportunities at All Levels: Interactions Among Operating Systems, Compilers, and Multicore Processors*, ACM SIGOPS Operating System Review. Volume 43, Issue 2. April 2009.
11. Bushra Ahsan and **Mohamed Zahran**, *Managing Off-Chip Bandwidth: A Case for Bandwidth-Friendly Replacement Policy*, in The 2nd Workshop on Managed Multi-Core Systems (MMCS'09), held in conjunction with ASPLOS 2009.
12. **Mohamed Zahran** and Sally A. McKee, *Adaptive Block Placement Policy for Cache Hierarchies* , in 3rd Workshop on statistical and Machine learning approaches to Architectures and compilaTion (SMART'09), held in conjunction with HiPEAC'09.
13. Bushra Ahsan and **Mohamed Zahran**, *Cache Performance, System Performance, and Off-Chip Bandwidth... Pick any Two*, in 3rd workshop Interconnection Network Architectures: On-Chip, Multi-Chip (INA-OCMC), held in conjunction with HiPEAC 2009.

14. Yufu Zhang, Ankur Srivastava and **Mohamed Zahran**, *Chip Level Thermal Profile Estimation Using On-chip Temperature Sensors*, Proc. International Conference on Computer Design (ICCD08), October 2008.
15. **Mohamed Zahran**, *Cache Replacement Policy Revisited*, in The Annual Duplicating, Deconstructing, and Debunking (WDDD) held in conjunction with the International Symposium on Computer Architecture (ISCA), 2007.
16. **Mohamed Zahran**, Kursad Albayraktaroglu, and Manoj Franklin, *Non-Inclusion Property in Multi-Level Caches Revisited*, in the International Journal of Computers and Their Applications, Special Issue on Techniques and Architectures for High Performance and Energy Efficient Computing Systems, Vol 14, Num 2, June 2007.
17. **Mohamed Zahran**, *Cache Hierarchy for 100 On-Chip Cores*, Fifth Annual Boston Area Architecture (BARC), Jan 2007.
18. **Mohamed Zahran**, *On Cache Blocks Behavior*, in International Computer Engineering Conference (ICENCO), Dec 2006.
19. **Mohamed Zahran** and Manoj Franklin, *RHT: A Context-Based Return Address Predictor*, in The 2006 International Conference on Computer Design (CDES'06), Las Vegas, June 2006.
20. **Mohamed Zahran** and Anasua Bhowmik, *Bandwidth-Friendly Cache Hierarchy*, in The 2006 International Conference on Computer Design (CDES'06), Las Vegas, June 2006.
21. **Mohamed Zahran** and Anasua Bhowmik, *Hybrid Compiler and Microarchitecture Technique for Cache Traffic Optimization*, in Interaction between Compilers and Computer Architectures (INTERACT 9), Feb 2005.
22. Francois Cantonnet, Yiyi Yao, **Mohamed Zahran** and Tarek El-Ghazawi, *Productivity Analysis of the UPC Language*, in 3rd International Workshop on Performance Modeling, Evaluation, and Optimization of Parallel and Distributed Systems (PMEO-PDS), to be held in conjunction with the International Parallel and Distributed Processing Symposium (IPDPS 2004).
23. **Mohamed Zahran** and Manoj Franklin, *Dynamic Thread Resizing for Speculative Multithreaded Processors*, in International Conference on Computer Design (ICCD), San Jose, CA, October, 2003. (**BEST PAPER AWARD**)
24. **Mohamed Zahran**, Manoj Franklin and Renju Thomas, *Confidence Estimation for Register Value Communication in Speculative Multithreaded Architectures*, in first value prediction workshop (VPW1), held in conjunction with the 30th Annual International Symposium on Computer Architecture (ISCA), San Diego, California, 2003.
25. **Mohamed Zahran**, *On Cache Memory Hierarchy for Chip-Multiprocessor*, in MEDEA workshop held in conjunction with PACT 2002 Conference, Charlottesville, Virginia, 2002. Also Appeared in ACM Computer Architecture News, Vol 31, No. 1, March 2003.
26. **Mohamed Zahran** and Manoj Franklin, *Return Address Prediction in Speculative Multithreaded Environments*, in Int'l Conference on Hi-Performance Computing (HiPC'02), Bangalore, India, 2002.
27. **Mohamed Zahran** and Manoj Franklin, *A Feasibility Study of Hierarchical Multi-threading*, in International Parallel and Distributed Processing Symposium (IPDPS 2002), Marriott Marina, Fort Lauderdale, Florida, 2002.
28. **Mohamed Zahran** and Manoj Franklin, *Hierarchical Multi-threading For Exploiting Parallelism at Multiple Granularities*, Workshop on MULTITHREADED EXECUTION, ARCHITECTURE and COMPILATION (MTEAC-5), Austin, Texas, 2001.

29. **Mohamed Zahran**, Ashraf Abdel-Wahab and Samir Shaheen, *Adaptive Genetic Algorithm for Multiprocessor Scheduling*, poster presentation at the Genetic and Evolutionary Computation Conference (GECCO), Orlando, 1999.

Refereed Posters, Abstracts, Invited Papers, and Technical Reports:

1. Arun K. Kanuparthi, **Mohamed Zahran**, and Ramesh Karri, *On-Chip Dynamic Trusted Platform Module*, Trusted Infrastructure Workshop (TIW), June 2010, Pittsburgh, PA, **Best Poster Award**.
2. **Mohamed Zahran** and Sally A. McKee, *Enterprise-Like Cache Hierarchy Management in the Manycore Era*, position abstract, ACM SIGPLAN Workshop on Memory Systems Performance and Correctness (MSPC) held in conjunction with ASPLOS, March, 2008.
3. Bushra Ahsan, Fatma Omara and **Mohamed Zahran**, *Chip Multiprocessor: Challenges and Opportunities*, INFOS 2008. (Invited Paper)
4. Jerry Backer and **Mohamed Zahran**, *The Effect of Memory Bandwidth on Processor Performance*, poster at Richard Tapia Conference, FL 2007 (**Winner of ACM SRC Grand Final**).
5. Bushra Ahasan and **Mohamed Zahran**, *Cache Improvement Techniques Reconsidered: A Write-Buffer Case Study*, poster at Richard Tapia Conference, FL 2007.
6. A. Bhowmik and **M. Zahran**, *Cache Traffic Optimization*, Computer Science and Automation, Indian Institute of Science, India, 2005, IISc-CSA-TR-2005-1.
7. **Mohamed Zahran**, *On Cache Memory Hierarchy for Chip-Multiprocessor*, ACM Computer Architecture News, Vol 31, No. 1, March 2003.

PRESENTATIONS
& TALKS

1. *Off-Chip Bandwidth: The New Wall in The Multicore Era*, Computer and Information Sciences Departmental seminar series, University of Delaware, March 2009.
2. *Multicore Chips and The Green Revolution*, IT Symposium by Uptime Institute, April 2009.
3. *Off-Chip Bandwidth: The New Wall in The Multicore Era*, Intel-VSSAD, Hudson, MA, May 2009.
4. *Adaptive Block Placement Policy for Cache Hierarchies* in SMART'09, held in conjunction with HiPEAC'09.
5. *Cache Performance, System Performance, and Off-Chip Bandwidth... Pick any Two*, INA-OCMC, held in conjunction with HiPEAC'09.
6. *Enterprise-Like Cache Hierarchy Management in the Manycore Era*, ACM SIGPLAN Workshop on Memory Systems Performance and Correctness (MSPC) held in conjunction with ASPLOS, March, 2008.
7. *Attacking The Von-Neumann Bottleneck: Cache Hierarchy in The Chip Multiprocessor Era*, as part of the departmental seminar series of Fall 2007, the ECE/CS dept of Polytechnic University.
8. *Attacking The Von-Neumann Bottleneck: Cache Hierarchy in The Chip Multiprocessor Era*, as part of the departmental seminar series of Fall 2007, the ECE dept, university of Massachusetts at Amherst.
9. *Cache Replacement Policy Revisited*, The Annual Workshop on Duplicating, Deconstructing, and Debunking (WDDD) held in conjunction with the International Symposium on Computer Architecture (ISCA), 2007.

10. *Attacking the Von-Neumann Bottleneck: Smart and Scalable Cache Hierarchy in The Chip Multiprocessor Era*, IBM T. J. Watson, Feb 2007.
11. *Computer Hardware: A Different Perspective*, keynote speech, 2nd International Computer Engineering Conference (ICENCO), Dec 2006.
12. *RHT: A Context-Based Return Address Predictor*, The 2006 International Conference on Computer Design (CDES'06), Las Vegas, June 2006.
13. *Bandwidth-Friendly Cache Hierarchy*, The 2006 International Conference on Computer Design (CDES'06), Las Vegas, June 2006.
14. *Chip Multithreading: Issues and Challenges*, part of the departmental seminar series of fall 2005 in the ECE dept, university of Massachusetts at Amherst.
15. *Cache Traffic Optimization and Cache on Demand System*, at a meeting at NSF with CSR program directory Prof. Peter Varman, June 2005.
16. *Hybrid Compiler and Microarchitecture Technique for Cache Traffic Optimization*, INTERACT-9 (Interaction between Compilers and Computer Architectures), Feb 2005.
17. *Confidence Estimation for Register Value Communication in Speculative Multithreaded Architectures*, first value prediction workshop (VPW1), held in conjunction with the 30th Annual International Symposium on Computer Architecture (ISCA), San Diego, California, 2003.
18. *Speculative Multithreading...The Future of Microprocessors*, Electrical and Computer Engineering Graduate Students Association (ECEGSA) Graduate Student Seminar, Fall 2002, **BEST SCIENTIFIC TALK AWARD**
19. *Microprocessors...Can We Make Further Progress*, University of Maryland Graduate Research Interaction Day (GRID), Spring 2002, **BEST TALK AWARD**
20. *On Cache Memory Hierarchy for Chip-Multiprocessor*, MEDEA workshop, held in conjunction with PACT, Virginia, 2002.
21. *Feasibility Study of Hierarchical Multithreading*, IPDPS Conference, Florida, 2002.

GRANTS

◇ External Funding:

- NSF-SGER 2007/2008: "SGER: Exploring the Potential for Software-Informed Hardware Reconfigurability in the Memory Hierarchy of Embedded Systems" (\$ 40,000).
- NSF-CBET 2007-2010, "MRI: Acquisition of an advanced micro-Computed Tomography imaging facility", (\$ 339,450) [Co-PI].
- CRA-CREU 2007/2008, Computing Research Association, title: "Toward Better Memory Hierarchy for Chip-Multiprocessor", (\$9,500).
- CRA-CREU 2006/2007, Computing Research Association, title: "Effect of Bus Traffic on Cache Hierarchy Performance", (\$3,500).

◇ Internal Funding:

- PSC-CUNY grant 40 (2009/2010), The Professional Staff Congress-City University of New York award for research on *Off-Chip Bandwidth Management for Multicore Processors*, (\$2,700).
- PSC-CUNY grant 38 (2007/2008), The Professional Staff Congress-City University of New York award for research on *Global Replacement Policy*, (\$3,950).
- PSC-CUNY grant 36 (2005/2006), The Professional Staff Congress-City University of New York award for research on *Improving Cache Memory Performance in Current and New Microarchitecture Environments* (\$2,320).

PROFESSIONAL
ACTIVITIES

◇ **Program committee member:**

- The 25th International Conference on Supercomputing (ICS-2011)
- The 24th IEEE International Parallel and Distributed Processing Symposium (IPDPS-2010)
- The International Symposium on Code Generation and Optimization (CGO-2010)
- The Fourth international Workshop on Automatic Performance Tuning (iWAPT 2009)
- The 11th IEEE International Conference on High Performance Computing and Communications (HPCC-09)
- The 2nd International Conference on Computer Science and its Applications (CSA 2009)
- IEEE International Conference on Microelectronics (ICM) 2007, 2008, and 2009
- The International Computer Design Conference (CDES-2006)

◇ **Editorial**

Co-guest editor for a special issue of ACM Operating System Review about The interaction among Compilers, Operating Systems, and Multicore; April 2009.

◇ **Organizing Committee Member:**

- Publication Chair for Computing Frontiers 2011
- Workshops and tutorials co-chair for the 23rd International Conference on Supercomputing (ICS 2009)
- Publicity chair for the Eighteenth International Conference on Parallel Architectures and Compilation Techniques (PACT 2009)
- Co-organizer of 2nd Reconfigurable and Adaptive Architecture Workshop (RAAW), held in conjunction of The 40th Annual IEEE/ACM International Symposium on Microarchitecture, Dec 2007.
- Co-organizer of 1st Reconfigurable and Adaptive Architecture Workshop (RAAW), held in conjunction of The 39th Annual IEEE/ACM International Symposium on Microarchitecture, Dec 2006.

◇ **Reviewing activities:**

- Reviewer for Air Force Office of Scientific Research
- IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems
- ACM Transactions on Architecture and Code Optimization (TACO)
- IEEE Computer Architecture Letters
- Journal Of Circuits, Systems, and Computers
- Journal of Computers and Their Applications
- International journal of embedded systems (IJES)
- International Conference on Supercomputing (ICS)
- International Symposium on Computer Architecture (ISCA)
- International Symposium on High Performance Computer Architecture (HPCA)
- International Symposium on Circuits and Systems (ISCAS)
- International Parallel and Distributed Processing Symposium (IPDPS)
- International Conference on High Performance Computing (HiPC)
- IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS)

Mohamed Zahran

- International Computer Engineering Conference (ICENCO).

- SOCIETIES AND AFFILIATIONS
- ◇ Full Member of Sigma Xi Honor society since 2002
 - ◇ Senior member of IEEE (including Computer Society).
 - ◇ Member of the following IEEE Computer society technical committees :
 - Computer Architecture (TCCA)
 - Microprocessors and MicroComputers (TCMCMP)
 - Microprogramming and Microarchitecture (TCMARCH)
 - ◇ Senior Member of ACM.
 - ◇ Member of the following ACM Special Interest Groups (SIG) :
 - Computer Architecture (SIGARCH)
 - Microprogramming (SIGMICRO)
 - Operating Systems (SIGOPS)
 - Computer Science Education (SIGCSE)
 - Design Automation (SIGDA)
 - Programming Languages (SIGPLAN)
 - ◇ Member of Egyptians Syndicate Professional Engineers society, since 1997.

- TEACHING EXPERIENCE
- ◇ **Graphics Processing Units (GPUs): Architecture and Programming** (Spring 2012)
In Computer Science Department of New York University
A graduate course that studies GPUs from hardware and software perspective.
 - ◇ **Compilers Construction:** (Spring 2010, Fall 2010, Spring 2011, Spring 2012) In Computer Science Department of New York University
A graduate course in compilers design, that involves building a full compiler.
 - ◇ **Capstone Project:** (Fall 2007, Spring 2008, Fall 2008, Spring 2009)
In Electrical Engineering Department at City College of City University of New York
Supervising several senior design projects, including: interfacing, software tool to help computer architecture researchers, and microprocessor design
 - ◇ **Digital Computer Systems** (Spring 2005, Fall 2005, Spring 2006, fall 2006, Spring 2007, Fall 2007, Spring 2008, Fall 2008, Spring 2009, Fall 2009, Spring 2010) In Electrical Engineering Department at City College of City University of New York
This is a senior-level course about computer architecture.
 - ◇ **Computer Engineering Laboratory:** (Fall 2004)
In Electrical Engineering Department at City College of City University of New York
This senior-level lab consists of several hands-on experiments in interfacing and FPGA.
I have also been faculty co-ordinator for that course (Spring 2005, Fall 2005, Spring 2006, and fall 2006)
 - ◇ **Co-Teaching Graduate Course in Computer Architecture:** (Spring 04)
Advanced graduate course in computer architecture and microprocessor design
In ECE department at The George Washington University
Duties include helping in preparing the syllabus, exams, projects, and giving lectures.
 - ◇ **Teaching assistant:** (Fall 99 - Spring 01)
In ECE department, University of Maryland at College Park. Assisted in teaching: Digital Logic Design, Computer Organization.
Duties: holding weekly recitation classes, office hours as well as grading homework assignments and exams.

Mohamed Zahran

- ◇ **Assistant Lecturer** (Sep 97 - May 99)
Cairo University, Egypt.
Teaching: C programming language, Digital Logic Design,
Computer Architecture, Software Engineering and Operating Systems.
- ◇ **Lecturer** (Spring 98)
Center of Adult and Continuing Education (CACE),
American University in Cairo (AUC).
Duties: Teaching computer architecture and assembly language programming course.

ADVISING

- ◇ **Ph.D. Adviser of:**
 - Bushra Ahsan, Dissertation Title: *Off-Bandwidth for Multicore Processors: The Next Big Wall*, First employment: postdoc at University of Cyprus in 2010/2011; Now at Intel Hudson, MA.
- ◇ **Ph.D committee member of the following students:**
 - Ahmed Elkammar, City University of New York, August 2007
 - Zahidur Rahman, City University of New York, June 2007
 - Zhaoming Li, City University of New York, May 2007
 - Qiang Song, City University of New York, May 2007
 - Hassan Bajwa, City University of New York, Apr 2007
 - Flavio De Angelis, City University of New York, 2005
 - Kafi Hassan, City University of New York, 2005.
 - Osama Hussein, City University of New York, 2005.
 - Hooshang Sharif, City University of New York, 2005.
- ◇ **M.Sc. committee member of the following Students:**
 - Hassan Bajwa, City College of City University of New York, Feb 2006
 - Jonathan Cardenas, City College of City University of New York, Dec 2005
 - Francois Cantonnet, ECE Dept, The George Washington University, Spring 04.
- ◇ **Supervisor of M.Sc. students for their M.Sc. report:**
 - Artem Durytskyy, ECE Department, Polytechnic Institute of NYU, (Spring 2011)
 - Lakshmi Cuddalore Arivudainambi, City College of City University of New York, (Fall 2007)
 - Preethi Gopinath, City College of City University of New York, (Fall 2007)
 - Sravan Paruchuri, City College of City University of New York, (Spring 2007)
 - Gurpreet Kaur, City College of City University of New York, (Spring 2007)
 - Bhaveshkumar Patel, City College of City University of New York, (Spring 2007)
 - Khurram Malik, City College of City University of New York, (Spring 2007)
 - Sandy Sakani, City College of City University of New York, (fall 2006)
 - Prasanna Uday Patil, City College of City University of New York, (fall 2006)
 - mattupalli susheela, City College of City University of New York, (fall 2006)
 - Varun Kumar Yadav Nalla, City College of City University of New York, (fall 2006)
 - Qasim Ali Mir, City College of City University of New York, (fall 2006)
 - Babji Reddy, City College of City University of New York, (fall 2006)
 - Mehul shah, City College of City University of New York, (summer 2006)

- Pramod Yadav, City College of City University of New York, (spring 2006)

◇ **Supervisor of undergraduate research of:**

- Abhi Kumar (Spring 2009)
- Lina Cordero (Fall 2007)
- Heba Gabre(Fall 2007)
- Stephany Soria (Fall 2007)
- Jumie Yuventi(Fall 2007)
- Jerry Backer (Spring 2007, Fall 2007)
- Elbert Tsang (Fall 2006)
- Rajai Gooden (Spring 06)
- Mamadou Lame (Fall 05)
- Juan P. Monzon (Spring 05-Fall 05)
- Ruhul Amin (Spring 05)
- Mahfuzur Rahman (Spring 05)

RESEARCH
SUMMARY

◇ **Dynamic Trusted Platform Modules**(2010-present)

Trusted Platform Module (TPM) is a module placed on-board to provide load-time authentication of general purpose computing systems. This project has three goals. The first is to extend TPM to provide *trusted* execution of programs, and not be limited to load-time or boot-time. The second is to solve the scalability issues of TPMs. The third goal is to embed TPMs into multicore and manycore chips for tighter interaction with the different cores.

◇ **Cache Hierarchy Extremely Scalable and Smart (CHESS)** (2006-present)

In this project, we design the cache hierarchy for many-core chips (i.e. more than 100 on-chip cores). The desired hierarchy must allow cores to exchange information in a fast way, even during very short cycle time, while decreasing off-chip bandwidth requirement. This requires rethinking of many aspects of cache design such as the interaction among caches and the bandwidth wall, the need for a global replacement and placement policy, and the hierarchical decision making in cache hierarchy.

◇ **Chip Multithreading**(2004-2010)

As the number of transistors has already exceeded billion transistors per chip, the inclusion of several processing elements per chip is now feasible. Making the best use of this chip-multiprocessing capability is a challenging problem. To achieve that goal, we study problems such as: dynamic balancing between high throughput and high single-thread performance, fast and dynamic pattern detection of different application behaviors, dynamic reconfiguration of several processing elements on-chip, and the continuous interaction between the compiler and architecture for better dynamic optimization

◇ **Reconfigurable and Parallel Architecture:**(2003-2004)

In this project, we study the integration of both general-purpose processors as well as reconfigurable engines in order to allow the machine to dynamically reconfigure itself based on run-time information to achieve the performance of an ASIC with the flexibility of a general purpose machine. Moreover, the project involves the design of language extension to the C-programming language for shared memory architectures. The language is called Unified Parallel C (UPC).

◇ **Hierarchical Multithreading** (1999-2003)

This is a new execution model I proposed in my Ph.D thesis that makes use of speculative multithreading in a novel way. It is used to parallelize a sequential program using a combined hardware and software approaches.